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Dated: 10-23-03

Signature:  (Yayoi Isaacson)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

David LEWIS et al.

Serial No.: Not Yet Assigned

Filing Date: Concurrently Herewith

For: ARITHMETIC STRUCTURES FOR
PROGRAMMABLE LOGIC DEVICES

Examiner: Not Yet Assigned

Group Art Unit: Not Yet Assigned

**INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97 & 1.98**

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, Applicants submit for consideration in the above-identified application the documents listed on the attached Form PTO-1449. The Copies of the documents are also submitted herewith (items 44-56). The items 1-43 are not enclosed. The U. S. Patent and Trademark Office waives the requirement under 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U. S. patent for all U. S. national patent applications filed after June 30, 2003. The Examiner is requested to make these documents of record.

This Information Disclosure Statement is submitted:

- ☒ With the application; accordingly, no fee or separate requirements are required.
- ☐ Within three months of the application filing date or before mailing of a first Office Action on the merits; accordingly, no fee or separate requirements are required.
- ☐ After receipt of a first Office Action on the merits but before mailing of a final Office Action or Notice of Allowance.
 - ☐ A fee is required. A check in the amount of * is enclosed.
 - ☐ A fee is required. Accordingly, a Fee Transmittal form (PTO/SB/17) is attached to this submission in duplicate.
 - ☐ A Certification under 37 C.F.R. § 1.97(e) is provided below; accordingly, no fee is believed to be due.
- ☐ After mailing of a final Office Action or Notice of Allowance, but before payment of the issue fee.
 - ☐ A Certification under 37 C.F.R. § 1.97(e) is provided below and a check in the amount of * is enclosed.
 - ☐ A Certification under 37 C.F.R. § 1.97(e) is provided below and a Fee Transmittal form (PTO/SB/17) is attached to this submission in duplicate.

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

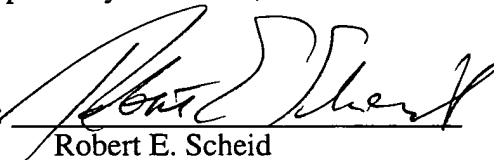
In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicants petition for

any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing 306812005300. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: October 23, 2003

Respectfully submitted,

By:



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Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>	Docket Number 306812005300	Application Number Not Yet Assigned
	Applicants David LEWIS et al.	
	Filing Date Concurrently Herewith	Group Art Unit Not Yet Assigned
	Mailing Date October 23, 2003	

U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
	1.	11/9/1993	5,260,610	Pedersen et al.			
	2.	11/9/1993	5,260,611	Cliff et al.			
	3.	12/28/1993	5,274,581	Cliff et al.			
	4.	3/15/1994	5,295,090	Hsieh et al.			
	5.	9/20/1994	5,349,250	New			
	6.	10/25/1994	5,359,242	Veenstra			
	7.	10/25/1994	5,359,468	Rhodes et al.			
	8.	11/15/1994	5,365,125	Goetting et al.			
	9.	7/25/1995	5,436,575	Pedersen et al.			
	10.	1/2/1996	5,481,206	New et al.			
	11.	1/9/1996	5,483,478	Chiang			
	12.	1/2/1996	5,481,486	Cliff et al.			
	13.	5/20/1997	5,631,576	Lee et al.			
	14.	1/16/1996	5,485,103	Pedersen et al.			
	15.	1/30/1996	5,488,316	Freeman et al.			
	16.	3/19/1996	5,500,608	Goetting et al.			
	17.	6/4/1996	5,523,963	Hsieh et al.			
	18.	8/13/1996	5,546,018	New et al.			
	19.	5/13/1997	5,629,886	New			
	20.	9/30/1997	5,672,985	Lee			
	21.	10/7/1997	5,675,262	Duong et al.			
	22.	3/3/1998	5,724,276	Rose et al.			
	23.	6/2/1998	5,761,099	Pedersen			

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EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.	
sf- 1587921 PTO/SB/ 08 (2-92)	
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE	

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	24.	10/6/1998	5,818,255	New et al.			
	25.	3/30/1999	5,889,411	Chaudhary			
	26.	4/27/1999	5,898,319	New			
	27.	4/27/1999	5,898,602	Rothman et al.			
	28.	6/1/1999	5,909,126	Cliff et al.			
	29.	7/6/1999	5,920,202	Young et al.			
	30.	7/20/1999	5,926,036	Cliff et al.			
	31.	12/7/1999	5,999,016	McClintock et al.			
	32.	2/1/2000	6,021,423	Nag et al.			
	33.	4/18/2000	6,051,992	Young et al.			
	34.	4/22/2000	6,107,827	Young et al.			
	35.	9/12/2000	6,118,300	Wittig et al.			
	36.	11/28/2000	6,154,052	New			
	37.	11/28/2000	6,154,053	New			
	38.	11/28/2000	6,154,055	Cliff et al.			
	39.	12/5/2000	6,157,209	McGettigan			
	40.	2/20/2001	6,191,610 B1	Wittig et al.			
	41.	2/20/2001	6,191,611 B1	Altaf			
	42.	9/11/2001	6,288,570 B1	New			
	43.	6/4/2002	6,400,180 B2	Wittig et al.			

FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO

OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner	Ref.	Title
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		Mailing Date October 23, 2003	

Initials	No.	
	44.	E. Ahmed et al., "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA '2000 Monterey Ca, pp. 3-12.
	45.	D. Cherepacha et al., "DP-FPGA: An FPGA Architecture Optimized for Datapaths", VLSI Design 1996, vol. 4, no. 4, pp. 329-343.
	46.	S. Kaptanoglu et al., "A new high density and very low cost reprogrammable FPGA architecture", FPGA '99 Monterey Ca, pp. 3-12
	47.	J. Rose et al., "Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency", J. of Solid-State circuits, vol. 25, no. 5, Oct. 1990, pp. 1217-1225.
	48.	J. L. Kouloheris et al., "FPGA Area versus Cell Granularity-Lookup Tables and PLA Cells", FPGA '92, pp. 9-14.
	49.	"FLEX 8000 Programmable Logic Device Family", Altera Corp. June 1999, ver. 10.01, pp. 349-364.
	50.	"FLEX 10K Embedded Programmable Logic Device Family", Altera Corp. March 2001, ver. 4.1, pp. 1-28.
	51.	"FLEX 6000 Programmable Logic Device Family", Altera Corp., March 2001, ver. 4.1, pp. 1-17.
	52.	"Mercury Programmable Logic Device Family", Altera Corp., March 2002, ver. 2.0, pp. 1-34.
	53.	"APEX 20K Programmable Logic Device Family", Altera Corp., February 2002, ver. 4.3, pp. 1-29.
	54.	"Virtex TM - II Platform FPGAs: Detailed Description", XILINX , Advance Product Specification, v2.1.1, 12/6/2002, pp. 1-40.
	55.	"Stratix FPGA Family Data Sheet", Altera Corp., Preliminary Information, Dec. 2002, ver. 3.0, pgs. 1, 11-19.
	56.	"ORCA® Series 2 Field-Programmable Gate Arrays", Data Sheet, Lattice Semiconductor Corp., Jan. 2003, title sheet, pp. 2-26.

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